We claim:

1. A method for making a heterojunction bipolar transistor, comprising:

(a) depositing a first polysilicon layer over shallow trench regions and a single crystalline SiGe intrinsic base region over a collector region;

(b) forming an oxide layer over the first polysilicon layer;

(c) forming a first nitride layer over the oxide layer;

(d) etching an opening through the first nitride layer, said opening corresponding to an emitter opening of said transistor;

(e) filling said emitter opening with a second polysilicon layer;

(f) forming an emitter pedestal from the second polysilicon layer and the first nitride layer, said emitter pedestal having a width which is wider than said emitter opening; and

(g) implanting source/drain implant regions into at least the first polysilicon layer, said source/drain implant regions being self-aligned with the second polysilicon layer in said emitter pedestal.

2. The method of claim 1, wherein the second polysilicon layer is in the shape of a T, with respective portions overlapping the first nitride layer.

3. The method of claim 2, wherein said step of forming said emitter pedestal includes making a length of the first SiGe polysilicon layer on one side of

said emitter pedestal and a length of the first SiGe polysilicon layer on another side of said emitter pedestal to be different lengths, and wherein the side with large length will be used as base contact.

4. The method of claim 1, wherein the first polysilicon layer is an SiGe layer.

5. The method of claim 4, wherein said SiGe layer is less than 0.15 um thick.

6. The method of claim 1, wherein said oxide layer is a high-pressure thermal oxide layer.

7. The method of claim 1, wherein said collector region is an n- epitaxy region on top of a sub-collector region.

8. The method of claim 1, wherein said step of forming said emitter pedestal includes making a length of the second polysilicon layer on one side of said emitter pedestal at least substantially equal to a length of the second polysilicon layer on another side of said emitter pedestal, said substantially equal lengths causing said transistor to have equal base resistances on said one side and said another side of said emitter pedestal.

9. The method of claim 1, wherein said source/drain implant regions are extrinsic base regions.

10. The method of claim 1, wherein said step of forming said emitter opening includes:

forming a TEOS layer over the first nitride layer;

forming an ARC layer over the TEOS layer;

forming a resist over the ARC layer;

developing the resist layer and forming patterns on the ARC layer;

etching through selective portions of the ARC layer and the TEOS layer; and

stripping the resist and ARC layers, wherein the TEOS layer is a hard mask to etch the nitride layer to form said emitter opening.

11. The method of claim 1, wherein said step of forming said emitter pedestal includes:

forming a second nitride layer over the second polysilicon layer;

forming a photoresist over the second nitride layer; and

etching away the second nitride layer, the second polysilicon layer, and the oxide layer except in a region underlying said photoresist.

12. The method of claim 11, further comprising:

varying photo tolerance during said step of forming said emitter pedestal to minimize mis-alignment between the second polysilicon layer in said emitter pedestal and said emitter opening.

13. A heterojunction bipolar transistor, comprising:

a collector region;

a SiGe base region;

an emitter stack overlying said collector region, said emitter stack including an emitter opening filled with T-shaped polysilicon, said T-shaped polysilicon overlying nitride regions included in said stack; and

extrinsic base regions arranged on respective sides of said emitter stack, said extrinsic base regions being aligned with said emitter polysilicon region but not being directly aligned with said emitter opening.

14. The transistor of claim 13, wherein said extrinsic base regions are made from SiGe polysilicon.

15. The transistor of claim 13, wherein one of said extrinsic base regions is longer than another of said extrinsic base regions, and wherein a base contact is formed on the longer extrinsic base region.

16. The transistor of claim 13, wherein said reach-through collector region, emitter stack, and extrinsic base regions are contacted using mid-end-of-line collector, emitter, and base contact contacts respectively.